Notice of Allowability	Application No.	Applicant(s)	
	10/697,717	D'ARCY ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt filed on 12/20/06*.

2. ☒ The allowed claim(s) is/are *1-16*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

Examiner's statement for reason for allowance

1. Claims **1-16** have been allowed.

The following is an examiner's statement for allowance:

As per claim 1:

The prior art (Henrikson Dana, U.S. PN: 6,324,670) of record teach a method and apparatus for generating a checksum that minimizes the creation and manipulation of carry bits by allowing a "running sum" to expand into a register having a larger capacity than the size of the message segments being processed. A checksum generator includes at least one adding circuit for processing a given message in segments and associated with the adding circuit is a register for temporarily holding the running sum that is being calculated by the adding circuit. A register is twice the size of the message segments being processed and is segregated into a high order portion and a low order portion (see col. 1, lines 60-67).

The prior art (Van Meter, III, Rodney, U.S. PN: 6,964,008) of record teach a method of generating checksum values for data segments retrieved from a data storage device for transfer into a buffer memory. The method includes the steps of maintaining a checksum list comprising a plurality of entries corresponding to the data segments stored in the buffer memory, each entry being for storing a checksum value for a corresponding data segment stored in the buffer memory (see col. 1, lines 54-67).

However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method of receiving a data block, partitioning the data

block into N segments of a data matrix, N being an integer greater than one, comparing N to a number of segments processed by each of at least two reduction stages, the at least two reduction stages arranged in a tree structure and If N is less than or equal to the number of segments processed by a highest level reduction stage, then processing the data matrix with a lowest level reduction stage that is configured to process the entire data matrix to generate a new data matrix, and repeating the said processing the data matrix with a lowest level reduction stage for each subsequent new data matrix until two data segments remain; otherwise, if N is greater than the number of segments processed by the highest-level reduction stage, then dividing the data matrix into one or more portions, processing one matrix portion with the highest-level reduction stage that is configured to process the matrix portion to generate a new data matrix, repeating the processing the data matrix with a lowest level reduction stage for each subsequent new data matrix until two data segments remain for each subsequent new data matrix of the one matrix portion until two data segments corresponding to the one matrix portion remain, appending another portion of the data matrix to the two data segments corresponding to the one matrix portion, and repeating if N is less than or equal to the number of segments processed by a highest level reduction stage until no matrix portions remain, combining the remaining two data segments to provide a checksum result and verifying the integrity of the received data block based on the checksum result. Consequently, claim 1 is allowed over the prior arts.

Claims **2-8,** which are directly or indirectly dependents of claim 1 are also allowed.

As per claim 9:

The prior art (Henrikson Dana, U.S. PN: 6,324,670) of record teach a method and apparatus for generating a checksum that minimizes the creation and manipulation of carry bits by allowing a "running sum" to expand into a register having a larger capacity than the size of the message segments being processed. A checksum generator includes at least one adding circuit for processing a given message in segments and associated with the adding circuit is a register for temporarily holding the running sum that is being calculated by the adding circuit. A register is twice the size of the message segments being processed and is segregated into a high order portion and a low order portion (see col. 1, lines 60-67).

The prior art (Van Meter, III, Rodney, U.S. PN: 6,964,008) of record teach a method of generating checksum values for data segments retrieved from a data storage device for transfer into a buffer memory. The method includes the steps of maintaining a checksum list comprising a plurality of entries corresponding to the data segments stored in the buffer memory, each entry being for storing a checksum value for a corresponding data segment stored in the buffer memory (see col. 1, lines 54-67).

However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious an apparatus comprising a processor adapted to coordinate processing of one or more reduction stages, at least two reduction stages arranged in a tree structure and each of the reduction stage configured to process a matrix, a combiner adapted to combine two remaining data segments to provide a result and further the apparatus is configured to receive the data block and verify the received data

block based on the checksum result provided by the combiner, and wherein the processor is configured to compare N segments of a data matrix representing the then, data block to a number of segments processed by each of the at least two reduction stages, N being an integer greater than one, and wherein the processor is adapted configured to coordinate a test if N is less than or equal to the number of segments processed by a highest level reduction stage then a lowest level reduction stage that is configured to process the entire data matrix processes the data matrix to generate a new data matrix, and each subsequent new data matrix is processed by one or more corresponding reduction stages until the two data segments remain; otherwise, if N is greater than the number of segments processed by the highest-level reduction stage, then: the processor divides the data matrix into one or more portions; the highest-level reduction stage that is configured to process one matrix portion processes the one matrix portion to generate a new data matrix, the processor enables repetition of the said processor divides the data matrix into one or more portions and the highest-level reduction stage is configured to process one matrix portion process the one matrix portion to generate a new data matrix for each subsequent new data matrix of the one matrix portion until two data segments corresponding to the one matrix portion remain, the processor appends another portion of the data matrix to the two data segments corresponding to the one matrix portion, and the test repeated the test until no matrix portions remain. Consequently, claim 9 is allowed over the prior arts.

Claims **10-15,** which are directly or indirectly dependents of claim 9 are also allowed.

As per claim 16:

The prior art (Henrikson Dana, U.S. PN: 6,324,670) of record teach a method and apparatus for generating a checksum that minimizes the creation and manipulation of carry bits by allowing a "running sum" to expand into a register having a larger capacity than the size of the message segments being processed. A checksum generator includes at least one adding circuit for processing a given message in segments and associated with the adding circuit is a register for temporarily holding the running sum that is being calculated by the adding circuit. A register is twice the size of the message segments being processed and is segregated into a high order portion and a low order portion (see col. 1, lines 60-67).

The prior art (Van Meter, III, Rodney, U.S. PN: 6,964,008) of record teach a method of generating checksum values for data segments retrieved from a data storage device for transfer into a buffer memory. The method includes the steps of maintaining a checksum list comprising a plurality of entries corresponding to the data segments stored in the buffer memory, each entry being for storing a checksum value for a corresponding data segment stored in the buffer memory (see col. 1, lines 54-67).

However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious a computer-readable medium having stored thereon a method and plurality of instructions executed by a processor cause the processor to implement a method for calculating a checksum for a data block, the method comprising the steps of method of receiving a data block, partitioning the data block into N segments of a data matrix, N being an integer greater than one, comparing N to a

number of segments processed by each of at least two reduction stages, the at least two reduction stages arranged in a tree structure and If N is less than or equal to the number of segments processed by a highest level reduction stage, then processing the data matrix with a lowest level reduction stage that is configured to process the entire data matrix to generate a new data matrix, and repeating the said processing the data matrix with a lowest level reduction stage for each subsequent new data matrix until two data segments remain; otherwise, if N is greater than the number of segments processed by the highest-level reduction stage, then dividing the data matrix into one or more portions, processing one matrix portion with the highest-level reduction stage that is configured to process the matrix portion to generate a new data matrix, repeating the processing the data matrix with a lowest level reduction stage for each subsequent new data matrix until two data segments remain for each subsequent new data matrix of the one matrix portion until two data segments corresponding to the one matrix portion remain, appending another portion of the data matrix to the two data segments corresponding to the one matrix portion, and repeating if N is less than or equal to the number of segments processed by a highest level reduction stage until no matrix portions remain, combining the remaining two data segments to provide a checksum result and verifying the integrity of the received data block based on the checksum result. Consequently, claim 16 is allowed over the prior arts.

CONCLUSION

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,591,397	Henrikson, Dana M
US PN: 6,968,498	Pal, Suprio
US PN: 6,964,008	Van Meter, III, Rodney
US PN: 6,643,821	Karim et al.
US PN: 6,412,092	Raghunath, Balakrishna
US PN: 6,324,670	Henrikson, Dana M.

3. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

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Art unit: 2133

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